Remarks and Arguments

In the Office Action dated 05/01/2008 ("Office Action"), Claims 1, 2, 6-16, 19-29, 36 and 37 were rejected, and Claims 3, 4, 17, 18, and 30-35 were objected to. In the Amendment set forth above, Claims 1, 4, 12, and 26 are amended, Claims 2 and 3 are cancelled and rewritten with Claim 1, Claim 5 was previously cancelled, and the remaining Claims are as previously or originally presented. In view of the amendments to the Claims and the Arguments and Remarks set forth below, reconsideration and reexamination are respectfully requested, and it is submitted that all Claims are in condition for Allowance.

1. The provisions of 35 U.S.C. §103(a) are duly noted.

2. The factual inquiries set forth in *Graham v. John Deere Co.* are duly noted.

3. The rejection of Claims 1, 2, 6-16, 19-29, and 36-37 under 35 U.S.C. §102(a) as being unpatentable over Lewis et al., U.S. Patent No. 4,201,337, in view of Usami, US patent 6,205,516, is respectfully traversed.

The Lewis system is summarized for discussion purposes. Lewis describes an error detection and correction (EDC) circuit that operates in either an error correction code (ECC) mode or a byte parity (BP) mode. When the EDC circuit has been configured to operate in ECC mode, the circuit uses a Hamming code to generate ECC check bits on data being stored to RAM. These check bits can then be used to detect, and possibly correct, errors when the data is later read from RAM. When the EDC circuit is instead configured to operate in BP mode, the EDC circuit is used to generate or verify byte parity on the data. The mode of operation is determined by a signal applied to an ECC/BP terminal of the Lewis circuit.

As has been previously explained in earlier prosecution, the Lewis system was developed at a time when data processing systems were constructed primarily of discrete components. The dual-mode operation of the Lewis EDC circuit was provided to fulfill "...the need to limit the number of LSI chip-types in a

data processing system." In other words, at one place in a given design, an instance of the EDC circuit (e.g., one LSI component) could be used in BP mode, and at a different point in the same design, a different instance of this same circuit (e.g., a different chip) could be configured in ECC mode. In this manner, the same chip-type was used in two different ways, thereby minimizing the number of chip-types maintained in a manufacturing inventory. This is described in reference to Lewis Figure 1, wherein instance 30a of the EDC circuit is said to be configured in ECC mode, and instances 30b-30f of this circuit are described as being used in BP mode.

It does not appear from Lewis that the same instance of the EDC circuit can be configured to operate in ECC mode at some times and to operate in BP mode at other times. That is, a given instance of an EDC circuit is configured to always operate in BP mode, or to always operate in ECC mode, and the functionality is not dynamically selectable.

From the foregoing description of the functionality of Lewis, it is clear that Lewis neither teaches nor suggests a system where the selection for treatment of data read from a memory between two different modes is determined by mode signals stored with the data signals.

While the Examiner asserts that Lewis teaches a circuit that is capable of operating in two different modes and recognizes that Lewis does not teach where the mode signal is supplied from and if and how it is stored, it is respectfully submitted that Lewis does not teach or suggest a dynamic system where one of two possible modes of treatment of data is determined by mode signals stored with the data signals.

The Examiner finds that Usami resolves the deficiency of Lewis by "teaching a programmable mode register which acts as a storage device to store a mode designator", and directs attention to col. 9, lines 45-62. While it may be conceded that Usami does teach a mode register, it must be understood that the functionality of the mode register of Usami is to establish control signals for the operation of the memory whereby the address data A0-A11 is provided as input data to the SDRAM together with control signals CS, RAS, CAS, and WE, for

controlling readout of the memory by controlling the column address counter. This control is accomplished by establishing control signals designating burst length, burst type, and the CAS latency. Clearly, Usami does not teach or suggest controlling mode selection, as taught and claimed by Applicant, that is responsive to mode signals associated with the data in storage. It is submitted, then, that Usami fails to supply teaching or suggestion that would alone or in combination with Lewis render the rejected Claims obvious.

Further, the combination of the teaching of Usami with that of Lewis is improper in that the mode selection required by Lewis is directed to enabling a common circuit type for one of two possible modes of operation as it relates to operation on the data, whereas Usami describes a mode register that is utilized to control the operation of the memory itself. The Examiner has failed to make any finding as to how the mode register of Usami could function with the memory system of Lewis.

The Examiner has not provided any finding as to why one skilled in the art would look to Usami to provide the type of mode control indicated by the Lewis system, wherein the mode register of Usami is utilized to control the readout function of the SDRAM when Lewis specifies mode control that is provided to control functionality of a common circuit type between two possible operations. Simply finding a reference that happens to refer to a "mode register", where the modes specified in Lewis and Usami are functionally independent of one another, does not support a prima facie case of obviousness. Rather it is a piecemeal attempt on a hindsight basis to put together teachings from diverse systems to attempt to show obviousness. This is not proper and is contrary to controlling law.

To support a legal conclusion of obviousness, as noted by the United States Supreme Court in ***KSR Int'l Co. v. Teleflex Inc.***, 550 U.S. ___(2007); 82 USPQ 2d 1385,

> "[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art."

Just because Lewis and Usami might or could be combined, does not render the combination proper under §103.

The ***KSR*** Court went on to state:

> "[it] can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." (Emphasis added)

Finally, the ***KSR*** opinion in favorably quoting ***In re Kahn,*** 441 F.3d 977, 988 (CA Fed. 2006) stated:

> "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (Emphasis added)

The Court made it clear that an obviousness rejection requires some articulated reason of why one skilled in the art would have been prompted to combine the elements in the claimed manner. It is respectfully submitted, that the reasoning provided by the Examiner for the combination of Lewis and Usami was arrived at on a hindsight basis, which is not permitted, rather than based upon a consideration of what one skilled in the art would have done at the time of the invention.

From the foregoing, then, it is currently controlling law that to establish an obviousness rejection, the Examiner is required to not only show that two or more references might or could be combined, but must identify reasons that would have prompted on of ordinary skill to have considered the combination. It is submitted that such a process has not been accomplished.

To combine the mode register and its functionality of Usami with the Lewis circuitry would appear to render the Lewis system inoperable in that the mode register of Usami is utilized to provide readout sequencing for the memory, whereas the Lewis system is directed to operating a common circuit type in two

different selectable modes. There has been no showing that the combined teaching would function as Lewis intended, nor is there any motivation to utilize the Usami mode register to control the Lewis memory in that Lewis is not concerned with controlling the memory per se, but is rather directed to utilizing a common circuit type in two different manners of operation to deal with data that is read from the memory. It would appear that the proposed modification of Lewis by the addition of Usami would render Lewis unsatisfactory for its intended purpose.

As noted in MPEP § 2143.01(v):

> **V. THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE**
>
> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USP 1125 (Fed. Cir. 1984) (Emphasis added)

In view of the foregoing, it is submitted that it cannot readily be argued that it would have been obvious to add the Usami mode register to the error detecting and correcting system contemplated by Lewis.

Finally, as noted above, the addition of the Usami mode register to Lewis would change the operation of Lewis by adding the Usami method of control of read out of the memory to the mode control defined by Usami. Lewis was not concerned about controlling the memory readout, but was rather concerned about selecting between two different error detecting systems to be applied to the data after it was read out. Such a modification would alter the operation of Lewis.

As noted in MPEP § 2143.01 (VI):

> **VI. THE PROPOSED MODIFICATION CANNOT CHANGE THE PRINCIPLE OF OPERATION OF THE REFERENCE**
>
> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)(Emphasis added)

As previously described, adding the Usami mode register and its principles of operation to Lewis would alter the principles of operation of Lewis; and, as such, is not permitted.

For the foregoing reasons it is respectfully submitted that the Examiner has failed to show a motivation to combine the teaching of Usami with that of Lewis; has failed to make any findings that the proposed combination of teachings would not alter the principles of operation of the primary reference; has failed to make any findings or showing that the proposed combinations of teachings would function; and, as result, has failed to make a *prima facie* case of obviousness in the rejection of the enumerated claims based upon the showing of Lewis in view of Usami.

Allowable Subject Matter

In paragraph 16 if the Office Action the Examiner has found Claims 3-4, 17-18, and 3-35 to include allowable subject matter, and stand rejected as being dependent upon rejected base claims, in paragraph 17 has provided reasons for this finding of allowable subject matter. The Examiner has stated that

> "No prior art teaches a storage device to store data signals wherein each of the addressable storage locations of the storage device stores data and a respective mode indicator to whether the circuit operates in the first or the second mode, the first mode interpreting data signals as control signals, and the second mode interpreting the data signals as error check signals."

Claims 1, 12, and 26 are the independent Claims in the Application, and each of them have been amended herein to reflect limitations that embody the allowable subject matter set forth above as determined by the Examiner in paragraph 17 of the Office Action. As to Claim 1, elements of dependent Claims 2 and 3 have been incorporated in Claim 1 and Claims 2 and 3 have been cancelled. Claim 4 is amended to reflect dependency from Claim 1 as amended. Claim 12 is a method Claim and has been amended such that the method steps recognize and incorporate the method steps reflecting the allowable subject

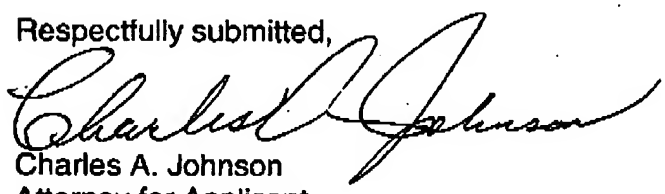
matter. Claim 26 is a means plus function Claim and has been amended to incorporate the allowable subject matter.

In view of the arguments and reasons set forth above and the Amendments made herein, Claims 1, 12, and 26 and all of the Claims that depend directly or indirectly from them are allowable as presently presented.

Conclusion

In the Office Action dated 05/01/2008, Claims 1-4 and 6-37 were pending, Claims 1, 2, 6-16, 19-29, 36 and 37 were rejected, and Claims 3, 4, 17, 18, and 30-35 were objected to as dependent from disallowed Claims. In the Amendment set forth above, Claims 1, 4, 12, and 26 are amended, Claims 2 and 3 are cancelled, and the remaining Claims are as originally or previously presented. In view of the amendments to the Claims and the Arguments and Remarks set forth herein, it is respectfully submitted that all Claims are in condition for Allowance, and a Notice of Allowance is respectfully requested. If the Examiner has any questions regarding the subject Application or this response, a call to the undersigned is encouraged and welcomed.

Respectfully submitted,



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